Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1-14. Canceled.

15 (Original). A transmission signal integrity supervisor, comprising:

a clock detector configured to receive a clock signal input and generate a first output signal in response to an at least one clock signal input anomalous condition; and a data supervisor configured to receive a digital data stream and generate a second output signal in response to an at least one digital data stream anomalous condition.

16 (Original). The signal integrity supervisor of claim 15, wherein the first output signal is a reset signal.

17 (Original). The signal integrity supervisor of claim 15, wherein the second output signal is a power down signal.

18 (Original). The signal integrity supervisor of claim 15, wherein the data supervisor receives a digital data stream from a delta-sigma modulator.

19 (Original). The signal integrity supervisor of claim 15, wherein the clock detector comprises a first monostable circuit and a second monstable circuit.

20 (Original). The signal integrity supervisor of claim 19, wherein the clock detector further comprises:

a current mirror; and

a resistor – capacitor combination having a resistance and a capacitance value respectively, selected such that the first output signal triggers in response to a clock signal input that falls below a minimum frequency.

21 (Original). The signal integrity supervisor of claim 15, wherein the data supervisor comprises:

a comparator; and

a maximum number counter.

22 (Original). The signal integrity supervisor of claim 21, wherein the comparator is configured to compare a data value from a previous clock cycle with a current data value and to generate a reset signal in response to consecutive data levels that vary.

23 (Original). The signal integrity supervisor of claim 21, wherein the maximum number counter is configured to increment upon detecting a clock cycle until it receives the reset signal from the comparator.

24 (Original). The signal integrity supervisor of claim 23, wherein the maximum number counter is configured to generate an output signal upon reaching a maximum count.

25 (Original). The signal integrity supervisor of claim 24, wherein the maximum number counter comprises a 4-bit asynchronous counter.

26 (Original). A circuit, comprising:

means for monitoring a digital data stream; and

means for generating an output signal in response to an anomalous condition in the digital data stream.

27 (Original). The circuit of claim 26, wherein the anomalous condition in the digital data stream would create a direct current (DC) transmit signal.

28 (Original). The circuit of claim 26, wherein the means for monitoring a digital data stream comprises a signal integrity supervisor.

29 (Original). The circuit of claim 28, wherein the signal integrity supervisor comprises a clock detector and a data supervisor.

30 (Original). The circuit of claim 28, wherein the means for generating an output signal is responsive to a digital data stream having a number of consecutive data values of equal magnitude wherein the number of consecutive data values reaches a predetermined maximum value.

31 (Original). The circuit of claim 28, wherein the means for generating an output signal is responsive to a digital data stream having a clock signal that falls below a predetermined minimum frequency.

32 (Original). A transmission unit, comprising: a signal integrity supervisor configured to generate a response to a digital data stream having an anomalous condition.

33 (Original). The transmission unit of claim 32, wherein the digital data stream anomalous condition is a clock signal frequency that falls below a predetermined minimum value.

34 (Original). The transmission unit of claim 32, wherein the digital data stream anomalous condition is a data signal having a corresponding data value that does not vary for a predetermined maximum number of clock cycles.

35-43. Canceled